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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/725,720	12/02/2003	Roy M. Zeighami	200300353-1	4318

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EXAMINER	
RUTLAND WALLIS, MICHAEL	
ART UNIT	PAPER NUMBER
2836	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/725,720	ZEIGHAMI ET AL.	
	Examiner	Art Unit	
	Michael Rutland-Wallis	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 February 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7-11 and 16-25* is/are pending in the application.

4a) Of the above claim(s) *16-27* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-10* is/are rejected.

7)☒ Claim(s) *11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election with traverse of election by original presentation of claims 7-11 in the reply filed on 02/21/2007 is acknowledged. The traversal is on the grounds that the process of using as claimed cannot be practiced with a material different process and no serious burden of search is present. This is not found persuasive because the method claimed (claims 7-11) state the limitation " setting via, a power selector circuit..." The product claims recite, "a power selector circuit to comprise a plurality of power selectors arranged in parallel". Therefore the product as claimed may be practiced with another materially different product such as a power selector without a plurality of power selectors arranged in parallel. Because these inventions are independent or distinct for the reasons given above and there would be a serious burden on the examiner if restriction were not required because the inventions have acquired a separate status in the art due to their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

The requirement is still deemed proper and is therefore made **FINAL**.

Response to Arguments

Applicant's arguments filed 02/21/2007 have been fully considered but they are not persuasive.

Response to 35 USC § 102 Arguments

Applicant's first allege a lacking of a teaching of "interfacing said plurality of power supplies with said electronic load through said power selector circuit" In support of this conclusion Applicant point out the loads shown are directly connected to the supply. In response the Office notes Applicant's assertion, however a direct connected between the supply and load does prohibit the "interfacing" of a switching circuit such as that shown in Foerster to redistribute power as the load conditions change. Applicant similarly points out this in the following page of the remarks "Foerster circuits operates to re-distribute that "excess current" to other loads using transformer 20 and switches ..." Clearly at least the arrangement of the switches translating and redistributing the power to the load constitutes an "interface" as claimed.

Applicant second assertion of a lack of "setting, via a power selector switch, a maximum effective voltage for each of said plurality of power supplies". In response, one should note cascade of parallel sources of Foerster is set form a maximum effective voltage (+18v) to a lowest effect voltage (-12v). Foerster points out as load conditions change load current may change as well, and discloses power form a first voltage bus acting a current sink may be switched to a second voltage bus acting a current source in order to balance the flow of power at various levels to minimize losses. Foerster discloses a selector circuit arranged between the source and the load, wherein said

selector circuit sets the maximum effective voltage supplied to the load by the translation and redistribution of power levels between loads, therefore the maximum effective voltage for the highest effective voltage (i.e. +18v) is supplied to the first load, a maximum effective voltage (+7v) is supplied to the second load, and the maximum effective voltage for lowest effective voltage (-12v) is supplied to the for the last of said plurality.

In view of the above Foerster teaches every claimed element, hence the rejection is deemed proper and therefore maintained.

Response to 35 USC § 103 Arguments

Applicant alleges with respect to claim 9 insufficient motivation to combine. Specifically citing "Foerster already operates to maximize the output to its loads". In response the Office contends Wasaki is provided to support the conclusion selecting or matching of impedance values is a known concept is the electrical power systems and most commonly utilized to minimize reflections and maximize the power supplied. Foerster teaches a switching system to minimize losses however the further inclusion of selecting or matching the impedance would still provide value to Foerster by reducing the needed switching of the system of Foerster.

Applicant's arguments, with respect to rejections of claims 10 and 11 under 35 USC § 103 Foerster in view of Chesavage have been fully considered and are persuasive. Therefore the rejection has been withdrawn.

Applicant alleges the rejection of Lethellier in view of Henze lack sufficient motivation to combine and does not teach every claimed limitation. Applicant specifically cites the motivation is lacking due to Lethellier already providing the correct voltage to the load. In response the Office first notes Lethellier supplies the correct voltage when all supplies are present when one supply is disconnected adjustments must be made in order to maintain the balance of power distributed to the load, secondly the Office notes that Lethellier is merely silent on the order in which the supplies are cascaded, where Henze is supplied to disclose a system teaching a cascade from high to low connecting the correct power to the loads, it remains the position of the Office the cascading from high to low of the supplied would have obvious to one of ordinary skill in the art at the time of the invention in order to arrange the system so the correct power is supplied to the load. Applicant also alleges Lethellier fails to teach "setting, via a power selector switch, a maximum effective voltage for each of said plurality of power supplies" citing there is nothing that indicates that the effective voltage of the power supply sets are controlled in any way. In response the Office points out Lethellier points out when a supply is removed or disconnected from the system the other supplies are controlled to supply power to the other loads to provide redundancy. Therefore the loads are in fact controlled.

In view of the above the rejections of Lethellier in view of Henze teach every claimed element and sufficient motivation to combine, hence the rejection is deemed proper and therefore maintained.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 7-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Foerster (U.S. Pat. No. 3,600,598)

With respect to claim 7 Foerster teaches a method for supplying power to an electronic load (seen in Fig. 2) comprising: connecting a plurality of power supplies in parallel (PS1-PS4); setting, via a power selector circuit (connection of current flow from power supply to load formed with diodes and/or switch means items 28, 32, 34 and 36 see col. 4 lines 19-37 describing the selection or distribution/redistribution of power), a maximum effective voltage for each of said plurality of power supplies to cascade from a highest effective voltage (PS1 +18 volts) for a first (PS1 for example) of said plurality to a lowest effective voltage (PS 4 -12 volts) for a last (PS4 for example) of said plurality; and interfacing (connection to supply power in Fig. 2) said plurality of power supplies with said electronic load through an said power selector circuit.

With respect to claim 8 Foerster teaches preventing current (see diodes in Fig. 2) generated by one of said plurality of power supplies from sinking into another of said plurality.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Foerster (U.S. Pat. No. 3,600,598) in view of Wasaki (U.S. Pub. No. 20030095036) Foerster teaches the process of claim 7, but does not teach the selecting an impedance to create said maximum effective voltage. Wasaki teaches the use of impedance matching circuits (items 20), the matching and selection of impedance values to deliver optimal power or maximum power to an electronic load. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Foerster to include the use of impedance selection to maximize the power output to the load.

Alternatively Claims 7 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lethellier (U.S Pat. No. 4,760,276) in view of Henze (U.S. Pat. No. 4,924,170)

With respect to claims 7 and 10 Lethellier teaches a method for supplying power to an electronic load comprising (Fig. 2 or 3): connecting a plurality of power supplies (PS1-PS3) in parallel; via a power selector circuit (via opening and closing of item 30), and interfacing said plurality of power supplies with said electronic load through an said

power selector circuit. Lethellier further teaches limiting said maximum effective voltage of one of said plurality of power supplies to a value of a next one of said plurality when said electronic load causes said maximum effective voltage of said one of said plurality to decrease to said maximum effective voltage of said next one of said plurality (see col. 4 lines 9-XX monitoring for a fault or addition of load). The arrangement of Lethellier uses variable resistors (item 20) and power selector (item 30) to equalize the output of the plurality of supplies (col. 3 lines 42-46) until some fault condition in the load or load change occurs (col. 4 lines 10-20) that supply may be isolated so that the problem may be resolved, and loads continue to operate based on the supply level of the adjacent supply (see col. 3 lines 47-53 where Lethellier described N+1 redundancy). Lethellier does not teach the cascading of supplies from highest voltage to lowest voltage as claimed in claim 1. Henze teaches the cascading of a highest effective voltage for a first of said plurality of power supplies to a lowest effective voltage for a last of said plurality of power supplies. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Lethellier in view of Henze to cascade the plurality of supplies in order of effective voltage in order to supply the correct voltage to the load.

Allowable Subject Matter

Claim 11 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The following is a statement of reasons for the

indication of allowable subject matter: the cited art teaches the limitations of claim 10 but fails to further teach reception of a signal to deactivated the limiting and deactivating said limiting. At least this further limitation to claim 10 is not rendered obvious by the prior art of record.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Rutland-Wallis whose telephone number is 571-272-5921. The examiner can normally be reached on Monday-Thursday 7:30AM-6:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2058. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MRW

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